International Journal of Advanced Technology and Innovative Research

ISSN 2348–2370
Vol.09,Issue.01,
January-2017,
Pages:0035-0044

www.ijatir.org

A Modified Controlling Approach for a Dual Unified Power Quality Conditioner

P.SUNIL KUMAR[1], P. SURENDRA BABU[2]

[1]Assistant Professor, Dept of EEE, Visvodaya Engineering College, Kavali, JNTUA, AP, India.
[2]PG Scholar, Dept of EEE, Visvodaya Engineering College, Kavali, JNTUA, AP, India.

Abstract: This paper presents a simplified control technique for a dual three-phase topology of a unified power quality conditioner - iUPQC. The iUPQC is composed of two active filters, a series active filter (SAF) and a shunt active filter (PAF) used to eliminate harmonics and unbalances. Different from a conventional UPQC, the iUPQC has the series filter controlled as a sinusoidal current source and the shunt filter controlled as a sinusoidal voltage source. Therefore, the PWM controls of the iUPQC deal with a well-known frequency spectrum, since it is controlled using voltage and current sinusoidal references, different from the conventional UPQC which is controlled using non-sinusoidal references. In this paper, the proposed design control, power flow analysis and experimental results of the developed prototype are presented.

Keywords: iUPQC, Power Flow Analysis, Shunt Active Filter (PAF), Series Active Filter (SAF).

I. INTRODUCTION

The usage of power quality conditioners in the distribution system network has increased during the past years due to the steady increase of nonlinear loads connected to the electrical grid. The current drained by nonlinear loads has a high harmonic content, distorting the voltage at the utility grid and consequently affecting the operation of critical loads. By using a unified power quality conditioner (UPQC) [1]– [32] it is possible to ensure a regulated voltage for the loads, balanced and with low harmonic distortion and at the same time draining undistorted currents from the utility grid, even if the grid voltage and the load current having harmonic contents. The UPQC consists of two active filters, the series active filter (SAF) and the shunt or parallel active filter (PAF) [1], [2]. The PAF is usually controlled as a non-sinusoidal current source, which is responsible for compensating the harmonic current of the load, while the SAF is controlled as a nonsinusoidal voltage source, which is responsible for compensating the grid voltage. Both of them have a control reference with harmonic contents and usually these references might be obtained through complex methods [4], [5], [14], [17], [21], [23], [27]. Some works shows a control technique to the both shunt and SAFs with uses sinusoidal references without the need of harmonic extraction, in order to decrease the complexity of the reference generation for the UPQC [31], [33].

An interesting alternative for power quality conditioners was proposed in [34] and was called Line Voltage Regulator/ Conditioner (LVRC). This conditioner consists of two single-phase current source inverters (CSI) where the SAF is controlled by a current loop and the PAF is controlled by a voltage loop. In this way, both grid current and load voltage are sinusoidal and therefore their references are also sinusoidal. Some authors have applied this concept, using voltage source inverters (VSI) in Uninterruptable Power Supplies (UPS) [35], [36] and in UPQC [10], [25], [32]. In [10] this concept is called “dual topology of unified power quality conditioner” (iUPQC), and the control schemes use the pq theory requiring determination in real time of the positive sequence components of the voltages and the currents. The aim of this paper is to propose a simplified control technique for a dual three-phase topology of a unified power quality conditioner (iUPQC) to be used in the utility grid connection. The proposed control scheme is developed in ABC reference frame and allows the use of classical control theory without the need for coordinate transformers and digital control implementation. The references to both SAF and PAFs are sinusoidal dispensing the harmonic extraction of the grid current and load voltage.
The paper is organized as follows. In Section II the iUPQC circuit is presented and its operation is explained in detail. Section III shows the power circuit design of the converters. The analysis and design of the passive filters are presented in Section IV. The proposed control scheme and its design are shown in Section V while the power flow is analyzed in Section VI. Section VII presents the experimental results and finally conclusions are drawn in Section VIII.

II. DUAL UNIFIED POWER QUALITY CONDITIONER

The conventional UPQC structure is composed of a SAF and a PAF, as shown in Fig. 1. In this configuration the SAF works as a voltage source in order to compensate the grid distortion, unbalances and disturbances like sags, swells and flicker. Therefore, the voltage compensated by the SAF is composed by a fundamental content and by the harmonics. The PAF works as a current source and it is responsible

IEEE Transactions on Industrial Electronics for compensate the unbalances, displacement and harmonics of the load current, ensuring a sinusoidal grid current. The series filter connection to the utility grid is made through a transformer, while the shunt filter is usually connected directly to the load, mainly in low voltage grid applications. The conventional UPQC has the following drawbacks: complex harmonic extraction of the grid voltage and the load involving complex calculations; voltage and current references with harmonic contents requiring a high bandwidth control; the leakage inductance of the series connection transformer affecting the voltage compensation generated by the series filter.

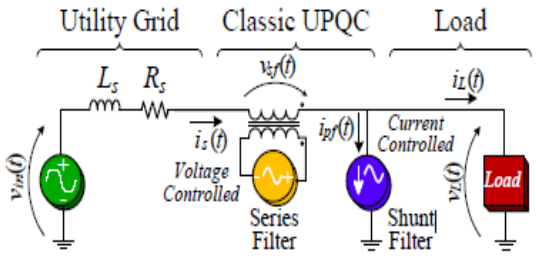

Fig. 1. Conventional Unified Power Quality Conditioner (UPQC).

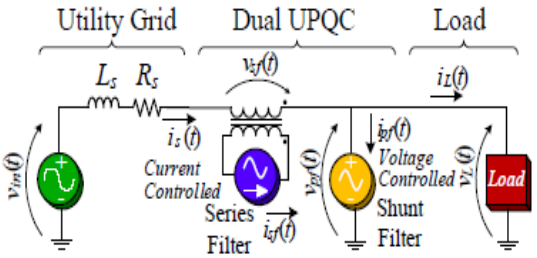

Fig. 2. Dual Unified Power Quality Conditioner (iUPQC).

In order to minimize these drawbacks, the iUPQC is investigated in this paper and its scheme is shown in Fig. 2. The scheme of the iUPQC is very similar to the conventional UPQC, using an association of the SAF and PAF, diverging only from the way the series and shunt filters are controlled. In the iUPQC the SAF works as a current source, which imposes a sinusoidal input current synchronized with the grid voltage. The PAF works as a voltage source imposing sinusoidal load voltage synchronized with the grid voltage. In this way, the iUPQC control uses sinusoidal references for both active filters. This is a major point to observe related to the classic topology since the only request of sinusoidal reference generation is that it must be synchronized with the grid voltage. The SAF acts as high impedance for the current harmonics, and indirectly compensates the harmonics, unbalances and disturbances of grid voltage since the connection transformer voltages are equals the difference between the grid voltage and load voltage. In the same way, thePAF indirectly compensates the unbalances, displacement and harmonics of the grid current, providing low impedance path for harmonic load current.

III. POWER CIRCUIT

The power circuit of the proposed iUPQC is made up of two four wire three-phase converters connected back-to-back and their respective output filters, as shown in Fig. 3

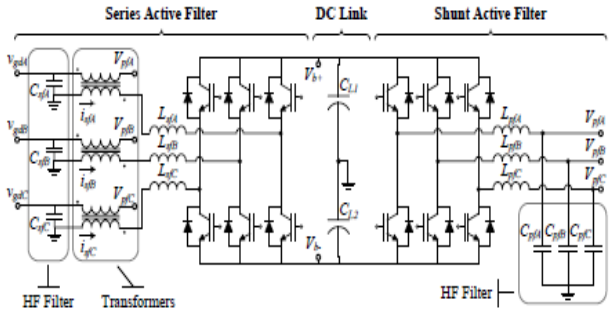

Fig. 3. Power circuit of the iUPQC.

TABLE I
DESIGN SPECIFICATIONS OF THE IUPQC

Input line-to-line RMS voltage	V_{in} = 220V
Output nominal power	P_o = 2500VA
DC link voltage	V_b = 400V
Utility grid frequency	f_{grid} = 60Hz
Switching frequency of series and PAFs	f_s = 20kHz
Transformer ratio	n = 1

TABLE II
COMPONENT SPECIFICATIONS OF THE POWER MODULES.

Leakage inductance of the SAF coupling transformers	L_{lg} = 2.33mH
Transformer ratio of the SAF coupling Transformers	n = 1
SAF connection inductance	L_{sf} = 650μH
PAF connection inductance	L_{pf} = 650μH
DC Link Capacitance	C_b = 3mF

Three single-phase transformers are used to connect the SAF to the utility grid while the PAF is connected directly to the load. Table I shows the specification of the iUPQC. For this work, a commercial back-to-back power module was used, manufactured by SEMIKRON. The passive components are shown in Table II.

IV. OUTPUT PASSIVE FILTER DESIGN

The iUPQC circuit can be analyzed by a single phase wiring diagram, as shown in Fig4. The utility grid impedance is represented by$Z_s = J\omega L_s + R_s$,while coupling transformer leakage impedance is represented by $Z_{lg} = J\omega L_g + R_{lg}$, and the voltage sources v_{sc} and v_{pc} represent the equivalent structures of the series and shunt filters, which generates a waveform composed by the fundamental component and by harmonics originated from the commutation of the switches. These high frequencies must be filtered by the output passive filters of the iUPQC ensuring sinusoidal grid currents and load voltages. Fig. 5

shows the equivalent circuit used for the SAF output impedance analysis and Fig. 6 shows the equivalent circuit used for the PAF output impedance analysis. In order to simplify the analysis of the PAF the voltage source v_{sc} and the inductance L_{sf} , which are series connected, were considered as a current source. Observing the equivalent circuits, we can claim that the PAF output impedance affects the frequency response of the SAF while the SAF output impedance does not affect the frequency response of the PAF.

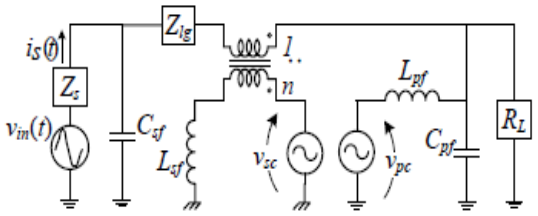

Fig. 4. Single phase wiring diagram of the dual UPQC.

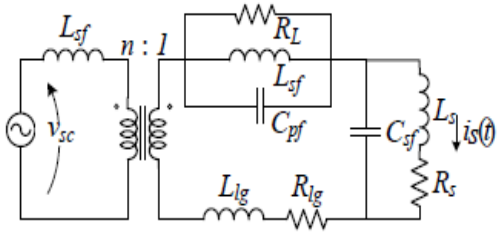

Fig. 5. Equivalent circuit as viewed by SAF.

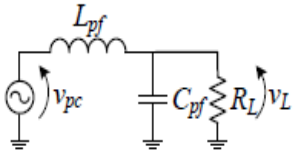

Fig. 6. Equivalent circuit as viewed by PAF.

Therefore the output passive filter design of the iUPQC should be started with the PAF design followed by the SAF design. The high frequency filter transfer function of the PAF is derived by analyzing the circuit of Fig. 6 and shown in Equation (1).

$$\frac{v_L(s)}{v_{pc}(s)} = \frac{1}{L_{pf}C_{pf}} \cdot \frac{1}{s^2 + s \cdot \frac{1}{C_{pf}R_L} + \frac{1}{L_{pf}C_{pf}}} \qquad (1)$$

The inductor L_{pf} was defined by the power design, so the capacitor C_{pf} will be defined according to the desired cutoff frequency for the filter. In this design, a 2.9kHz cutoff frequency was used, resulting in a value of 10_F for the C_{pf} filter capacitor. Fig. 7 shows the PAF frequency response for the nominal load and no-load. The high frequency filter transfer function of the SAF is derived by analyzing the circuit of Fig. 5 and shown in Equation (2).

$$\frac{i_s(s)}{v_{sc}(s)} = \frac{n}{\{sL_{sf} + n^2[sL_{lg} + R_{lg} + \alpha + \beta] \cdot \gamma\}} \qquad (2)$$

Where:

$$\alpha = \frac{sL_{pf}R_L}{s^2L_{pf}C_{pf}R_L + sL_{sf} + R_L} \qquad (3)$$

$$\beta = \frac{sL_{rd} + R_{rd}}{s^2L_sC_{sf} + sC_{sf}R_s + 1} \qquad (4)$$

$$\gamma = s^2C_{sf}L_s + sC_{sf}R_{lg} + 1 \qquad (5)$$

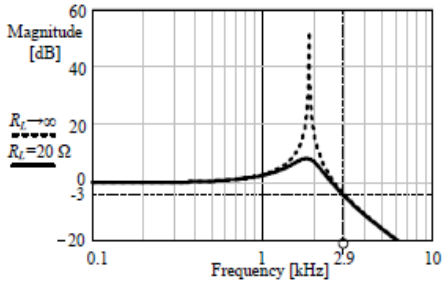

Fig. 7. The HF filter frequency response of the PAF.

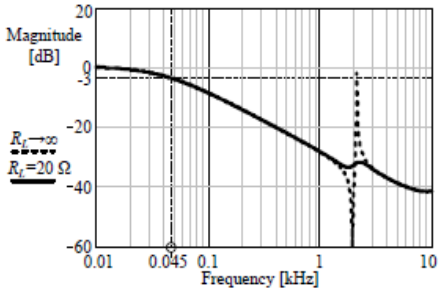

Fig. 8. The HF filter frequency response of the SAF.

As the inductor Lsf was defined by the power design, the capacitor Csf will be defined according to the desired cutoff frequency for the filter. In this design a 45Hz cutoff frequency was used, resulting in a value of 1_F for the Csf . Fig. 8 shows the SAF frequency response for nominal load and no-load. It can be noted than the filter response has a low cutoff frequency that can reduce the bandwidth of the SAF, decreasing its effectiveness under operation with harmonics contents on the grid voltage. This characteristic of low frequency attenuation is undesirable and intrinsic to the structure, due to the leakage impedance of the coupling transformers. An important contribution of this paper and different from what it was stated in some previous articles, which deal with the same iUPQC control strategy, is that in spite of the SAF operates with sinusoidal reference, the control of this filter needs to deal with high frequency since the current imposed by the SAF is obtained through the voltage imposition on this filter output inductor. The voltage imposed on these inductors is complementary to the utility grid voltage harmonics so that it guarantees a sinusoidal

current through the filter. Different from the conventional UPQC whose narrow band frequency control may distort the load voltage, in the iUPQC the narrow band frequency control may distort the current drained fromthe utility grid. The usage of high power coupling transformers, with low leakage inductance, and the design of higher voltage dc link, allowing the imposition of higher current rate of change on the filter output inductor, are solutions to change the characteristics of the filter attenuation in low frequencies.

V. PROPOSED CONTROL SCHEME

The proposed iUPQC control structure is an ABC reference frame based control, where SAF and PAF are controlled in an independent way.

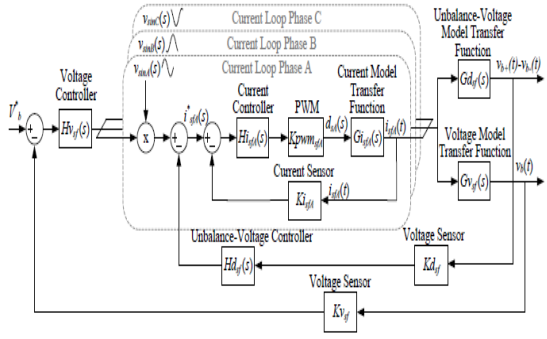

Fig. 9. Control block diagram of the SAF controller.

In the proposed control scheme, the power calculation and harmonic extraction are not needed since the harmonics, unbalances, disturbances and displacement should be compensated. The SAF has a current loop in order to ensure a sinusoidal grid current synchronized with the grid voltage. The PAF has a voltage loop in order to ensure a balanced, regulated, load voltage with low harmonic distortion. These control loops are independent one from each other since they act independently in each active filter. The dc link voltage control is made in the SAF where the voltage loop determines the amplitude reference for the current loop, in the same mode of the power factor converters (PFC) control schemes. The sinusoidal references for both SAF and PAF controls are generated by digital signal processor (DSP), which ensure the grid voltage synchronism using a phase-locked loop (PLL). A. SAF Control Fig. 9 shows the control block diagrams for the SAF. The SAF control scheme consists of three identical grid current loops and two voltage loops. The current loops are responsible for tracking the reference to each grid input phases, in order to control the grid currents independently. One voltage loop is responsible for regulating the total dc link voltage and the other is responsible for avoiding the unbalances between the dc link capacitors. The total dc voltage control loop has a low frequency response and determines the reference amplitude for the current loops.

Thus, when the load increases overcoming the input grid current, the dc link supply momently the active power consumption resulting in a decreasing of its voltage. This voltage controller acts to increase the grid current reference aiming to restore the dc link voltage. In the same way, when the load decreases, the voltage controller decreases the grid current reference to regulate the dc link voltage. Considering the three-phase input current, sinusoidal and balanced, the voltage loop transfer function is obtained through the method of power balance analysis. The three-phase four wire converter with neutral point can be represented by the circuit shown in Fig. 10, composed by a current source which is in parallel with the dc link impedance and whose current source represents the average charge current of dc link.

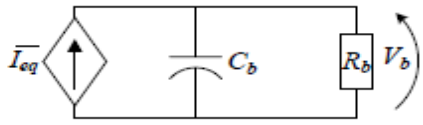

Fig. 10. Equivalent circuit of SAF voltage loop.

The resistor Rb is absent in the real circuit (Rb ! 1), it just represents instantaneous active power consumption of dc link. The term instantaneous is related to time of switching period, since active power consumption of dc link is null for utility grid voltage frequency. The average charge current of dc link is given by equation (6):

$$\overline{I_{eq}} = \frac{3}{2} \cdot \frac{n \cdot V_{gdpk} \cdot I_{sfpk}}{V_b}$$

The SAF peak current Isfpk is considered the same for the three phases due to balanced current. Through equation (6) the voltage loop transfer function is obtained and is represented
by equation (7):

$$Gv_{sf}(s) = \frac{V_b(s)}{I_{sf}(s)} = \frac{3}{2} \cdot n \cdot \frac{V_{gdpk}}{V_b} \cdot \frac{1}{\frac{1}{R_b} + sC_b} \qquad (7)$$

Where: Vgdpk - Peak of grid voltage; Vb - dc link voltage; Rb - load equivalent resistance; Cb - Total dc link equivalent capacitance; n - Transformer ratio; The open loop transfer function (OLTFv) is given by equation (8):

$$OLTFv(s) = Gv_{sf}(s) \cdot \frac{Kv_{sf}}{Ki_{sf}} \cdot Km_{sf} \qquad (8)$$

Where:
Kmfs - Multiplier gain; Kvsf - Voltage sensor gain; Kisf - Current sensor gain; The Kmfs gain is obtained considering the gain of the multiplier integrated circuit and the peak of the synchronized sinusoidal signal generated by DSP.

Aiming to regulate the total dc link voltage control, a proportional integral (PI) + pole controller was designed which ensures a crossover frequency of 4Hz and phase margin of 45_. The frequency response of the total voltage loop is shown in Fig. 11 including the open loop transfer function (OLTFv), controller transfer function (Hvsf) and the compensated loop transfer function (OLTFv + Hvsf). The unbalanced-voltage control loop also has a low frequency loop and acts on the dc level of the grid current reference in order to keep the voltage equilibrium in dc link capacitors. When a voltage unbalance occurs, this loop addsa dc level to the references of the grid currents aiming to equalize both CL1 and CL2 voltages.

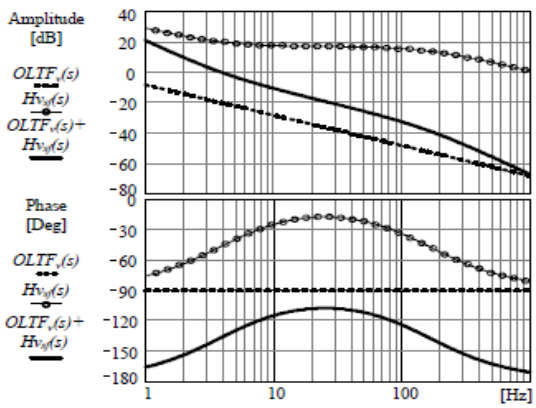

Fig. 11. Voltage loop frequency response of the SAF.

The unbalanced-voltage loop transfer function is obtained through the analysis of the simplified circuit shown in Fig. 12. The four wire converter allows the single-phase analysis, where two current sources represent the current on the inverter switches. In Fig. 12 the current isc(t) represents the current through the neutral point and d(t) represents the duty cycle. Through the mesh analysis and applying Laplace, the unbalanced-voltage loop transfer function is obtained andgiven by equation (9):

$$Gd_{sf}(s) = \frac{V_{b+}(s) - V_{b-}(s)}{I_{sc}(s)} = \frac{3}{2 \cdot s \cdot C_b} \qquad (9)$$

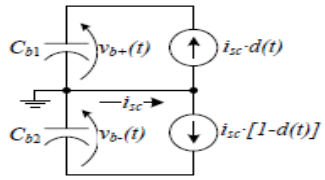

Fig. 12. Equivalent circuit of SAF unbalanced-voltage loop.

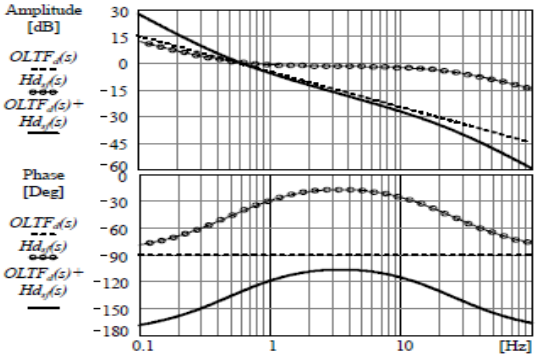

Fig. 13. Unbalance-Voltage loop frequency response of the SAF.

The open loop transfer function (OLTFd) is given by equation (10):

$$OLTF_d(s) = Gd_{sf}(s) \cdot \frac{Kd_{sf}}{Ki_{sf}} \qquad (10)$$

Where:

Kdsf - Differential voltage sensor gain; Aiming to eliminate the differential dc link voltage, a PI + pole controller was designed which ensures a crossover frequency of 0.5Hz and phase margin of 50_. The frequency response of the differential voltage loop is shown in Fig. 13, including the open loop transfer function (OLTFd), controller transfer function (Hdsf) and the compensated loop transfer function (OLTFd + Hdsf).

The current control scheme consists of three identical current loops, except for the 120 degree phase displacements from references of each other. The current loops have a fast response to track the sinusoidal references, allowing the decoupling analysis in relation to the voltage loop. The current loop transfer function is obtained through the analysis of the singlephase equivalent circuit shown in Fig. 14. The voltage source represents the voltage on the coupling transformer. The dynamic model is obtained through the circuit analysis using average values related to switching period. Under these conditions, the voltages vs(t) and vL(t) are constants. Through small signal analysis and using Laplace, the current loop transfer function is given by equation (11):

$$Gi_{fs}(s) = \frac{I_{sc}(s)}{D(s)} = \frac{V_b}{sA_1 + n^2 \cdot (R_s + R_{lg})} \qquad (11)$$

Where:

$$A_1 = n^2 \cdot (L_s + L_{lg}) + L_{sf} \qquad (12)$$

And:

Ls - Series grid inductance; Rs - Series grid resistance; Llg - Leakage inductance of the coupling transformer; Rlg - Series resistance of the coupling transformer; The open loop transfer function (OLTFi) is given by equation (13):

$$OLTFi(s) = Gi_{sf}(s) \cdot Kpwm_{sf} \cdot Ki_{sf} \qquad (13)$$

Where:

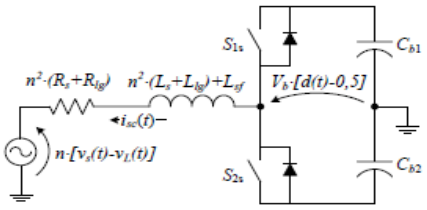

Fig. 14. Single-phase equivalent circuit of SAF.

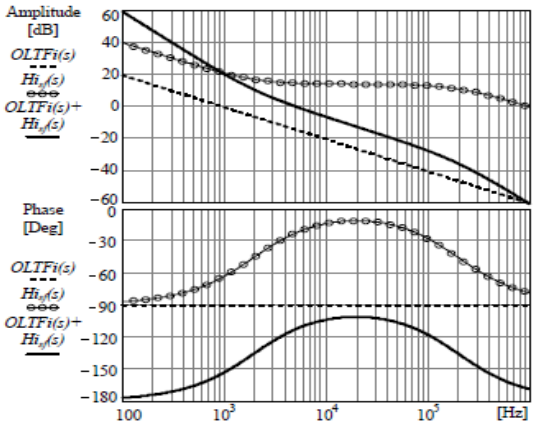

Fig. 15. Current loop frequency response of the SAF.

Kpwmsf - Series filter PWM modulator gain; The Kpwmsf gain equals the inverse peak value of the triangular carrier. Aiming to track the current reference, a PI + pole controllerwas designed which ensures a crossover frequency of 5kHz and phase margin of 70_. The frequency response of the current loop is shown in Fig. 15 including the open loop transfer function (OLTFi), controller transfer function (Hisf) and the compensated loop transfer function (OLTFi +Hisf).

B. PAF Control Fig. 16 shows the control block diagram of the shunt active filter controller.The PAF control scheme is formed by three identical load voltage feedback loops, except for the 120 degree phase displacements from references of each other. The voltage loops are responsible for tracking the sinusoidal voltage reference for each load output phases, in order to control the load voltages independently. The voltage loop transfer function is obtained through the analysis of the single-phase equivalent circuit show in Fig. 17. The dynamic model is obtained through the circuit analysis using average values related to switching period. Throughsmall signal analysis and using Laplace, the voltage loop transfer function is given by equation (14):

$$Gv_{pf}(s) = \frac{V_b}{L_{pf}C_{pf}} \cdot \frac{1}{s^2 + s\left(\frac{1}{C_{pf}R_L}\right) + \frac{1}{L_{pf}C_{pf}}} \qquad (14)$$

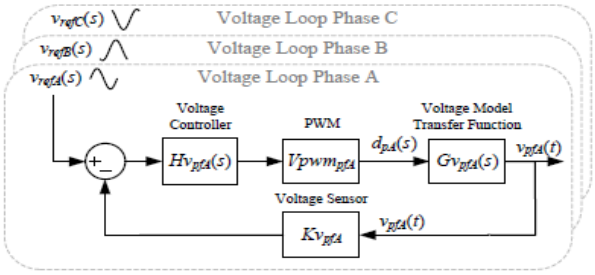

Fig. 16. Control block diagram of the PAF voltage loop.

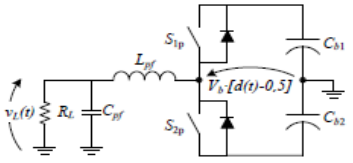

Fig. 17. Single-phase equivalent circuit of PAF.

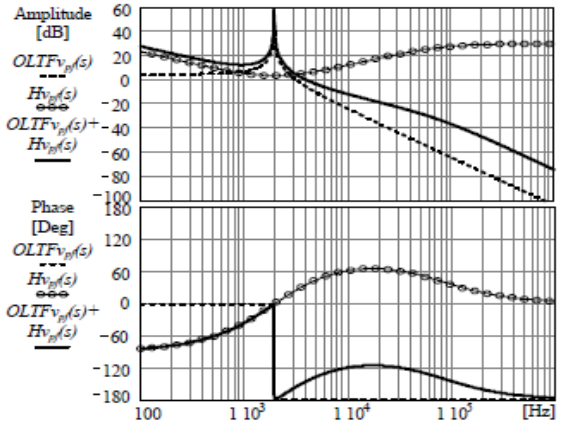

Fig. 18. Voltage loop frequency response of the SAF.

Where $Gv_{pf}(s) = V_L(s)/D(s)$.

The open loop transfer function ($OLTFv_{pf}$) is given by equation (15):

$$OLTFv(s) = Gv_{pf}(s) \cdot Kpwm_{pf} \cdot Kv_{pf} \qquad (15)$$

Where:

Kpwmpf - Shunt filter PWM modulator gain; Aiming to track the voltage reference, a proportional integral derivative (PID) + additional pole controller was designed which ensures a crossover frequency of 4kHz and phase margin of 35_. The voltage loop frequency response is shown in Fig. 18 including the open loop transfer function (OLTFvpf), controller transfer function (Hvpf) and the compensated loop transfer function (OLTFvpf + Hvpf).

VI. POWER FLOW

The active power flow of the iUPQC is shown in Fig. 19. In Fig. 19(a) the grid voltage vs has a lower amplitude than the

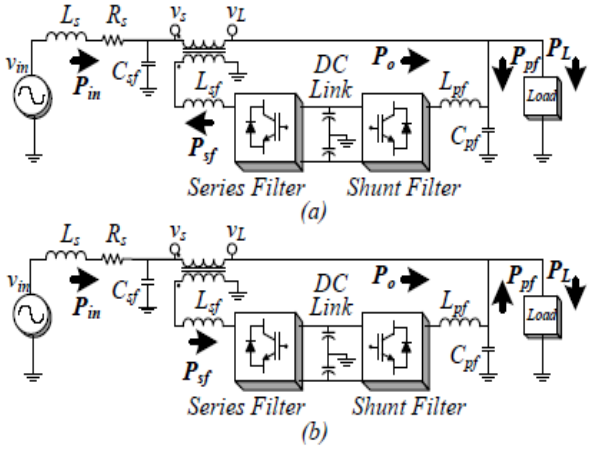

Fig. 19. Power flow of iUPQC; (a) $v_S < v_L$ (b) $v_S > v_L$.

load voltage vL. In this case, the SAF delivers active power to the load while the parallel active filter consumes active power. In Fig. 19(b) the grid voltage vs has a higher amplitude than the load voltage vL. In this case, the SAF consumes active power while the PAF filter delivers active power to the load. In an ideal situation when vs is equal to vL there is no active power flow through the SAF. The power drained from the electrical grid equals the sum of the load power and the iUPQC ower losses. In this paper, the output voltage vL is kept in phase with the fundamental component of the input voltage vin, thus the SAF operates with reactive power only when there are harmonics on the input voltage vin because the fundamental component of the coupling transformer voltage is always in phase with the current drained from the utility grid is. In steady state, assuming a sinusoidal and balanced utility grid voltage and disregarding the dual UPQC losses, the apparent power of SAF Ssf and PAF Spf normalized in relation to the apparent power of the load are given by Equations (16) and (17), respectively represented in Fig. 20 and Fig. 21.

$$\left|\frac{S_{sf}}{S_L}\right| = \frac{\cos\varphi_1 \cdot \sqrt{\left(1-\frac{V_L}{V_S}\right)^2}}{\sqrt{1+THDi^2}} \quad (16)$$

$$\left|\frac{S_{pf}}{S_L}\right| = \sqrt{\frac{\cos^2\varphi_1 \cdot \frac{V_L}{V_S} \cdot \left(\frac{V_L}{V_S}-2\right)}{1+THDi^2}+1} \quad (17)$$

Where cos('1) is the displacement factor and THDi is the total harmonic distortion of the output current. These equations are obtained through the analysis of the complex power of SAF _S sf and PAF _S pf .

$$\dot{S}_{sf} = \left(\dot{V}_s - \dot{V}_L\right) \cdot \dot{I}_s^* \quad (18)$$

$$\dot{S}_{pf} = \dot{S}_L - \dot{V}_L \cdot \dot{I}_s^* \quad (19)$$

Increasing THDi and decreasing cos('1), will decrease the ratio of jSsf=SLj and will increase the ratio of jSpf=SLj.

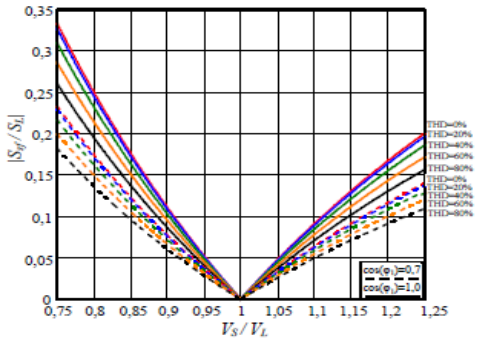

Fig. 20. Normalized apparent power of the SAF.

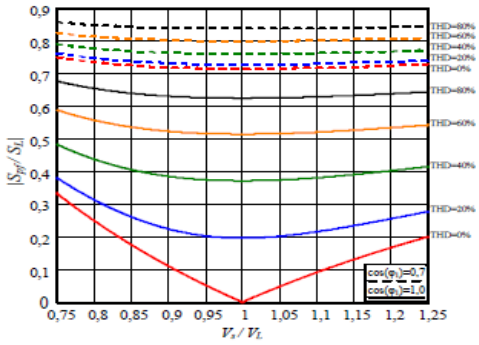

Fig. 21. Normalized apparent power of the PAF.

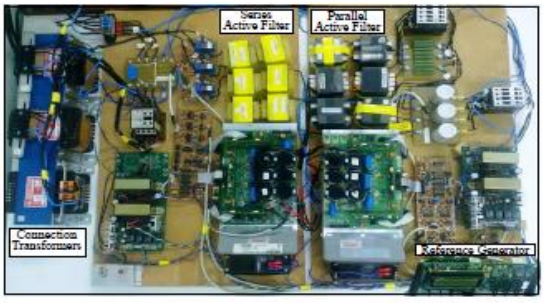

Fig. 22. The dual UPQC prototype.

This analysis shows it is possible to design a SAF with power capacity lower than nominal load power. By changing the transformers ratio it is possible to use power switches with lower current capacity. On the other hand, PAF is always designed for nominal load power since it has to process the total load reactive power.

VII. EXPERIMENTAL RESULTS

A 2500W prototype was built in order to obtain the experimental results for the proposed iUPQC. The prototype uses two back-to-back converters manufactured by SEMIKRON. The passive filters were designed according to the specifications of Table I. The prototype is shown in Fig. 22.

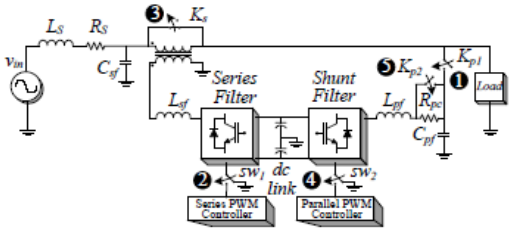

Fig. 23. Pre-charge sequence of iUPQC.

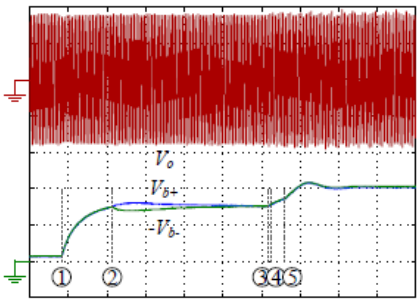

Fig. 24. dc link voltages (50V/div, 250ms/div) and load voltage (100V/div, 250ms/div) during pre-charge.

The pre-charge method and the pre-charge sequence is an important and not trivial design step of the iUPQC due to the power flow characteristics of the system. During the startup the voltage supplied to the load cannot be distorted and the iUPQC coupling in the circuit shall not affect the load. The pre-charge method developed allows the startup of the iUPQC with no need of load power disconnection. The used precharge sequence is shown in Fig. 23. The pre-charge circuit has three contactors, Ks, Kp1 and Kp2, and one in-rush resistor, Rpc. The switches sw1 and sw2 are used symbolically to show the switching turn-on time. The Kp1 and Kp2 contactors are initially opened, while the Ks contactor is initially closed and the switching of both active filters is initially disabled. The pre-charge sequence starts when the contactor Kp1 is turned on, providing the charge of dc link capacitors through anti-parallel diodes present in the PAF power circuit. After 340ms, the switching of the SAF sw1 is enabled, causing a voltage unbalance on dc link during a short period of time due to stabilization time of the SAF unbalance-voltage control loop. After 1sec, the Ks contactor is turned off, allowing the increase of the dc link voltage by SAF operation. After 10ms the switching of the PAF sw2 is enabled, starting the regulation of the load

voltage. After 100ms the Kp2 is turned on, finishing the pre-charge sequence. Fig. 24 presents the dc link voltage and the load voltage during the pre-charge sequence of the iUPQC. In order to emulate a harmonic distorted load current, it was used a three-phase rectifier with capacitive filter and two single-phase rectifiers with RL load connected to the phases A and B respectively.

In order to emulate a distorted grid voltage and evaluate the harmonic compensation of the grid voltage, a FCATH 450-38-50 Programmable AC Power Source manufactured by SUPPLIER Inc. was used. The power source supplies a threephase voltage source with 20% of third harmonic in phase A, 10% of fifth harmonic in phase B, and 10% of seventh harmonic in phase C. Fig. 25a shows the currents and voltages in the source and load. It is possible to see that the currents drained from the source are sinusoidal, balanced and synchronized with the source voltage, with a power factor of 0.980, 0.994 and 0.994 for the phases A, B, C respectively. The THDs of the load currents are 32.1%, 32.1% and 65.1% respectively, while the THDs of the source currents are 1.06%, 1.80% and 1.34%. The THDs of the source voltage equal 20.0%, 10.8% and 10.4% for phases A, B and C, respectively, while the load voltages have THDs equal to 0.53%, 0.69% and 0.38%, respectively. Fig. 25b shows the currents through the PAF. The PAF indirectly supplies the load harmonic currents because the SAF only drains the fundamental current component from the source. In a similar way Fig. 25c shows the voltages synthesized by the SAF. The SAF indirectly processes the harmonic grid voltages because the PAF imposes a synchronized sinusoidal voltage on the load. In order to verify the dynamic response of the iUPQC, Fig. 26a shows the source and the load voltages during a voltage interruption in phase A. Fig. 26b shows the source currents during a fault in phase A. It is possible to see that the source current in other phases have the amplitudes increased in order to keep the nominal power for the load. Fig. 26c shows the load voltages and the load currents during a load step from 50% to 100%. The load voltages and the load currents are shown in Fig. 26d during a load step from 100% to 50%. Fig. 26e shows the dc link voltages and the load current in phase A during a load step. The voltages in capacitors CL1 and CL2 remained balanced even during the load steps. The experimental results confirm the efficacy of the proposed scheme to control the iUPQC.

VIII. CONCLUSION

The results obtained with the iUPQC confirms that the proposed ABC reference frame control works very well and was able to compensating the nonlinear load currents and also ensure the sinusoidal voltage for the load in all three phases. The control also had a great performance during the load steps and voltage disturbances at the source.The main advantages of this proposed control in relation to other proposed schemes were the utilization of sinusoidal references for both series and shunt active filters controls without the need for complex calculations or coordinate transformations. The iUPQC references do not have harmonic contents and the only requirement is the synchronism with the grid voltage. Another positive aspect of the iUPQC in low voltage applications (distribution system network) is the non-interference of the leakage impedance voltage of the SAF connection transformer in the load voltage compensation, because the load voltage is directly controlled by the PAF. For other

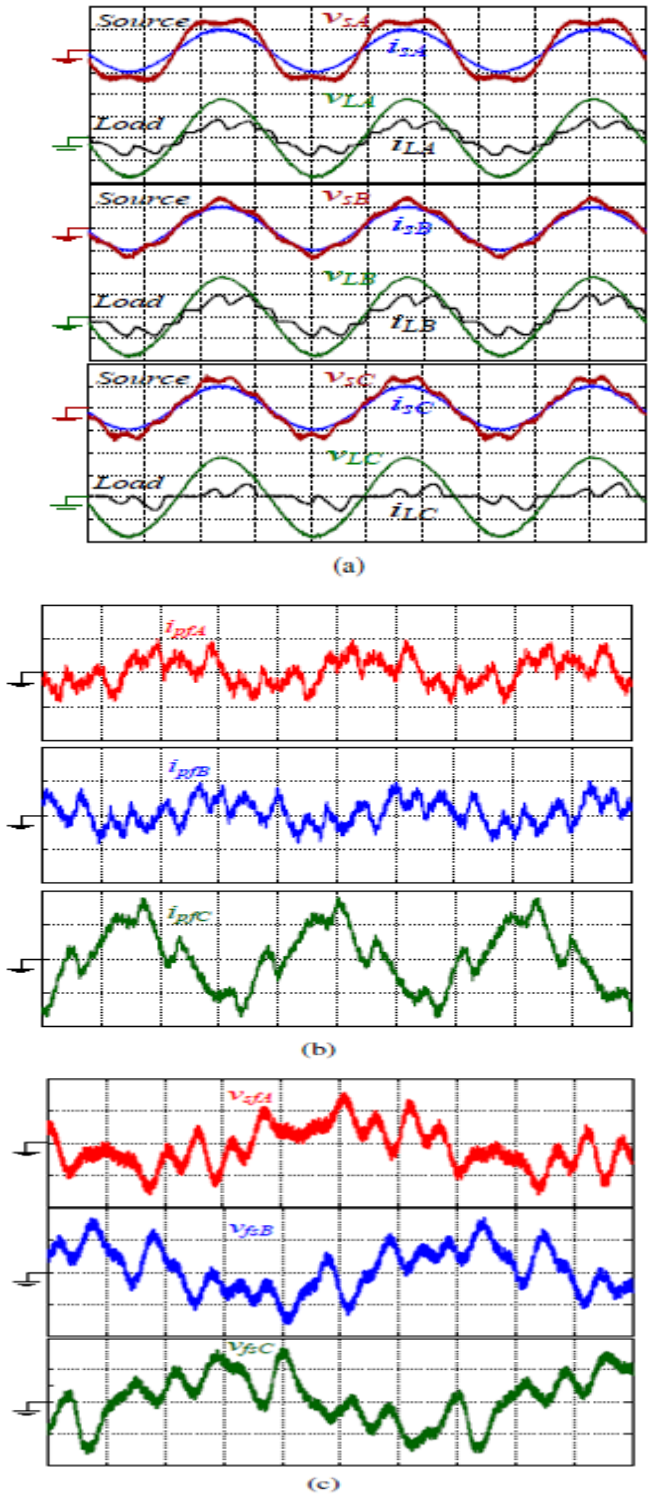

Fig. 25. (a) Source and load voltages (100V/div, 5ms/div), source and load currents (10A/div, 5ms/div). (b) PAF currents (6A/div, 5ms/div). (c) SAF voltages (30V/div, 2.5ms/div).

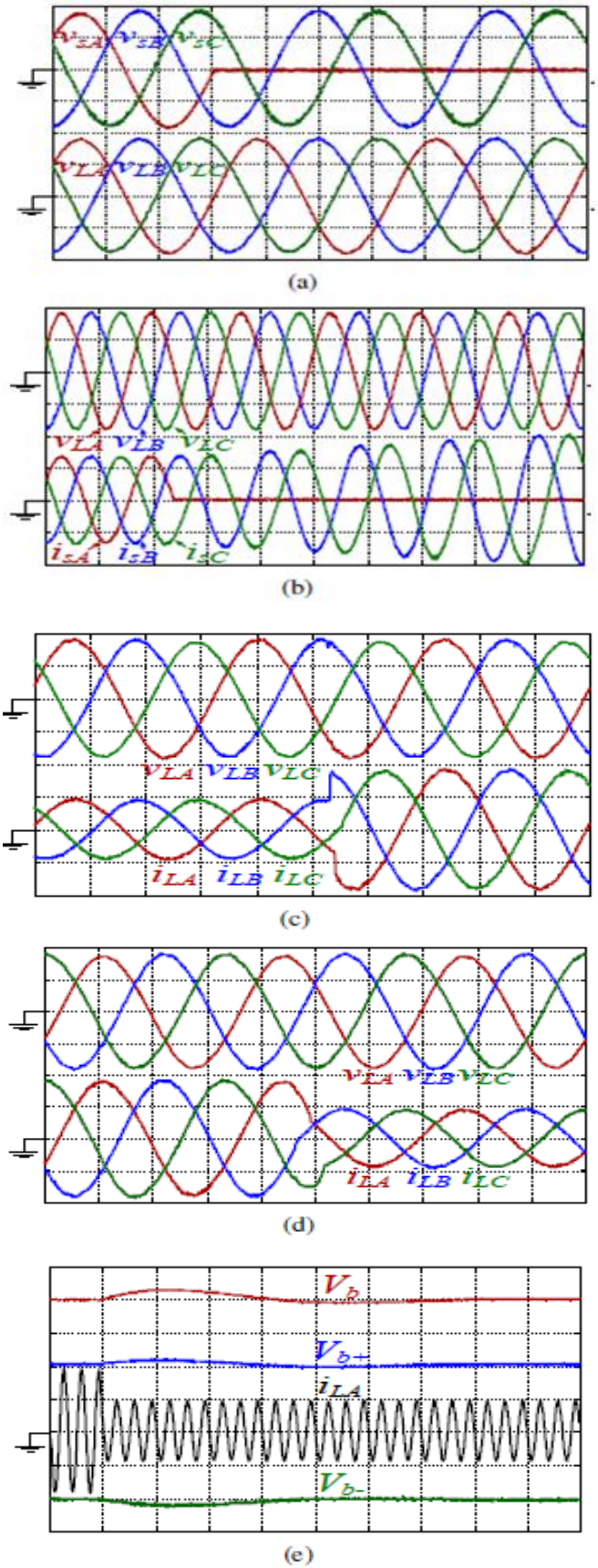

Fig. 26. (a) Source voltages and load voltages (100V/div, 5ms/div) during a voltage dip in phase A. (b) Load voltages (100V/div, 10ms/div) and source currents (5A/div, 10ms/div). (c) Load voltages (100V/div, 5ms/div) and load currents (5A/div, 5ms/div) during a load step from 50% to 100%. (d) Load voltages (100V/div, 5ms/div) and load currents (5A/div, 5ms/div) during a load step from 100% to 50%. (e) DC link voltages (100V/div, 50ms/div) and load current (5A/div, 50ms/div) during a load step from 100% to 50%. hand, the leakage impedance interferes in the current loop bandwidth, decreasing its frequency response under distorted grid voltages. The results validate the proposed iUPQC control scheme proving that the power quality can be meaningfully better with a simple control method which uses only synchronized sinusoidal references.

IX. REFERENCES

[1] M. Aredes, K. Heumann, and E. Watanabe, "An universal active power line conditioner," IEEE Trans. on Power Deliv., vol. 13, no. 2, pp. 545– 551, Apr 1998.

[2] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series and shunt-active filters," IEEE Trans. on Power Electron., vol. 13, no. 2, pp. 315–322, Mar 1998.

[3] B. Han, B. Bae, S. Baek, and G. Jang, "New configuration of upqc for medium-voltage application," IEEE Trans. on Power Deliv., vol. 21, no. 3, pp. 1438–1444, July 2006.

[4] S. Chakraborty, M. Weiss, and M. Simoes, "Distributed intelligent energy management system for a single-phase high-frequency ac microgrid," IEEE Trans. on Ind. Electron., vol. 54, no. 1, pp. 97–109, Feb 2007.

[5] M. Forghani and S. Afsharnia, "Online wavelet transform-based control strategy for upqc control system," IEEE Trans. on Power Deliv., vol. 22, no. 1, pp. 481–491, Jan 2007. [6] A. Jindal, A. Ghosh, and A. Joshi, "Interline unified power qualityconditioner," IEEE Trans. on Power Deliv., vol. 22, no. 1, pp. 364–372, Jan 2007.

[7] Y. Kolhatkar and S. Das, "Experimental investigation of a single-phase upqc with minimum va loading," IEEE Trans. on Power Deliv., vol. 22, no. 1, pp. 373–380, Jan 2007.

[8] M. Basu, S. Das, and G. Dubey, "Investigation on the performance of upqc-q for voltage sag mitigation and power quality improvement at a critical load point," IET Generation Transmission Distribution, vol. 2, no. 3, pp. 414–423, May 2008.

[9] V. Khadkikar and A. Chandra, "A new control philosophy for a unified power quality conditioner (upqc) to coordinate load-reactive power demand between shunt and series inverters," IEEE Trans. on Power Deliv., vol. 23, no. 4, pp. 2522–2534, Oct 2008.

[10] M. Aredes and R. Fernandes, "A dual topology of unified power quality conditioner: The iupqc," in 13th European Conf. on Power Electron. And Appl., Sept 2009, pp. 1–10.

[11] M. Brenna, R. Faranda, and E. Tironi, "A new proposal for power quality and custom power improvement: Open upqc," IEEE Trans. on Power Deliv., vol. 24, no. 4, pp. 2107–2116, Oct 2009.

[12] S. Chakraborty and M. Simoes, "Experimental evaluation of active filtering in a single-phase high-frequency ac microgrid," IEEE Trans. on Energy Conversion, vol. 24, no. 3, pp. 673–682, Sept 2009.
[13] V. Khadkikar and A. Chandra, "A novel structure for three-phase fourwire distribution system utilizing unified power quality conditioner(upqc)," IEEE Trans. on Ind. Appl., vol. 45, no. 5, pp. 1897–1902, Sept 2009.
[14] K. H. Kwan, Y. C. Chu, and P. L. So, "Model-based H1 control of a unified power quality conditioner," IEEE Trans. on Ind. Electron.,vol. 56, no. 7, pp. 2493–2504, July 2009.
[15] J. Munoz, J. Espinoza, L. Moran, and C. Baier, "Design of a modular upqc configuration integrating a components economical analysis," IEEE Trans. on Power Deliv., vol. 24, no. 4, pp. 1763–1772, Oct 2009.
[16] I. Axente, J. Ganesh, M. Basu, M. Conlon, and K. Gaughan, "A 12- kva dsp-controlled laboratory prototype upqc capable of mitigating
unbalance in source voltage and load current," IEEE Trans. on Power Electron., vol. 25, no. 6, pp. 1471–1479, June 2010.
[17] I. Axente, M. Basu, M. Conlon, and K. Gaughan, "Protection of unified power quality conditioner against the load side short circuits," IET Power Electron., vol. 3, no. 4, pp. 542–551, July 2010.
[18] S. Karanki, M. Mishra, and B. Kumar, "Particle swarm optimizationbased feedback controller for unified power-quality conditioner," IEEETrans. on Power Deliv., vol. 25, no. 4, pp. 2814–2824, Oct 2010.
[19] W. C. Lee, D. M. Lee, and T.-K. Lee, "New control scheme for a unified power-quality compensator-q with minimum active power injection," IEEE Trans. on Power Deliv., vol. 25, no. 2, pp. 1068–1076, April 2010.
[20] B. Franca and M. Aredes, "Comparisons between the upqc and its dual topology (iupqc) in dynamic response and steady-state," in IECON 37th Annu. Conf. on IEEE Ind. Electron., Nov 2011, pp. 1232–1237.
[21] M. Kesler and E. Ozdemir, "Synchronous-reference-frame-based control method for upqc under unbalanced and distorted load conditions," IEEE Trans. on Ind. Electron., vol. 58, no. 9, pp. 3967–3975, Sept 2011.
[22] V. Khadkikar and A. Chandra, "Upqc-s: A novel concept of simultaneous voltage sag/swell and load reactive power compensations utilizing series inverter of upqc," IEEE Trans. on Power Electron., vol. 26, no. 9, pp. 2414–2425, Sept 2011.
[23] V. Khadkikar, A. Chandra, A. Barry, and T. Nguyen, "Power quality enhancement utilising single-phase unified power quality conditioner: digital signal processor-based experimental validation," IET Power Electron., vol. 4, no. 3, pp. 323–331, March 2011.
[24] V. Kinhal, P. Agarwal, and H. Gupta, "Performance investigation of neural-network-based unified power-quality conditioner," IEEE Trans. on Power Deliv., vol. 26, no. 1, pp. 431–437, Jan 2011.
[25] A. Leon, S. Amodeo, J. Solsona, and M. Valla, "Non-linear optimal controller for unified power quality conditioners," IET Power Electron., vol. 4, no. 4, pp. 435–446, April 2011.
[26] V. Khadkikar, "Enhancing electric power quality using upqc: A comprehensive overview," IEEE Trans. on Power Electron., vol. 27, no. 5, pp. 2284–2297, May 2012.
[27] K. H. Kwan, P. L. So, and Y. C. Chu, "An output regulation-based unified power quality conditioner with kalman filters," IEEE Trans. on
Ind. Electron., vol. 59, no. 11, pp. 4248–4262, Nov 2012.
[28] G. Li, F. Ma, S. Choi, and X. Zhang, "Control strategy of a cross-phaseconnected unified power quality conditioner," IET Power Electron., vol. 5, no. 5, pp. 600–608, May 2012.
[29] J. Munoz, J. Espinoza, C. Baier, L. Moran, E. Espinosa, P. Melin, and D. Sbarbaro, "Design of a discrete-time linear control strategy for a multicell upqc," IEEE Trans. on Ind. Electron., vol. 59, no. 10, pp. 3797–3807, Oct 2012.
[30] K. Karanki, G. Geddada, M. Mishra, and B. Kumar, "A modified threephase four-wire upqc topology with reduced dc-link voltage rating," IEEE Trans. on Ind. Electron., vol. 60, no. 9, pp. 3555–3566, Sept 2013.
[31] J. Dias, T. D. C. Busarello, L. Michels, C. Rech, and M. Mezaroba, "Unified power quality conditioner using simplified digital control," SOBRAEP Trans., vol. 16, p. 9, 2011.
[32] K. Dai, P. Liu, G. Wang, S. Duan, and J. Chen, "Practical approaches and novel control schemes for a three-phase three-wire series-parallel compensated universal power quality conditioner," in APEC '04 Appl. Power Electron. Conf. and Expo., vol. 1, 2004, pp. 601–606 Vol.1.
[33] F. Pottker de Souza and I. Barbi, "Single-phase active power filters for distributed power factor correction," in PESC Power Electron. Spec. Conf., vol. 1, 2000, pp. 500–505 vol.1.
[34] S. Moran, "A line voltage regulator/conditioner for harmonic-sensitive load isolation," in Conf. Rec. IEEE Ind. Appl. Annu. Meeting., Oct 1989,pp. 947–951 vol.1.
[35] F. Kamran and T. Habetler, "A novel on-line ups with universal filtering capabilities," IEEE Trans. on Power Electron., vol. 13, no. 3, pp. 410– 418, May 1998.
[36] S. da Silva, P. Donoso-Garcia, P. Cortizo, and P. Seixas, "A three-phase line-interactive ups system implementation with series-parallel active power-line conditioning capabilities," IEEE Trans. on Ind. Appl., vol. 38, no. 6, pp. 1581–1590, Nov 2002.

Author's Profile:

P.Surendra Babu is currently PG scholar of EEE in power Electronics in Visvodaya Engeneering college, Kavali, Nellore(Dist), Affiliated to JNTU Anantapur.

P.Sunil Kumar, M.Tech working as Assistant Professor in the department of EEE at Visvodaya Engeneering college, Kavali, Nellore(Dist), Affiliated to JNTU Anantapur . He is dedicated to teaching field from the last 7 years.