Implementation of Power Efficient Vedic Multiplier

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Abstract: In this Paper, Urdhva tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This is shown to be very similar to the popular array multiplier architecture. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier structures. Nikhilam Sutra is then discussed and is shown to be much more efficient in the multiplication of large numbers as it reduces the multiplication of two large numbers to that of two smaller ones. The proposed multiplication algorithm is then illustrated to show its computational efficiency by taking an example of reducing a 4X4-bit multiplication to a single 2X2-bit multiplication operation. This work presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics.

Keywords: Vedic Multiplier, Xilinx, Efficiency.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulator(MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier.

II. IMPLEMENTATION

A. Algorithm For 4 X 4 Bit Vedic Multiplier Using Urdhva Tiryakbhyam(Vertically And Crosswise) for Two Binary Numbers

Line diagram for multiplication of two 4-bit numbers.

Fig.1.
Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position. Next, all the four bits are processed with crosswise multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage multiplication and addition of three bits except the LSB. The same operation continues until the multiplication of the two MSBs to give the MSB of the product. For example, if in some intermediate step, we get 110, then 0 will act as result bit (referred as r0) and 11 as the carry (referred as cn). It should be clearly noted that cn may be a multi-bit number with being the final product. Hence this is the general mathematical formula applicable to all cases of multiplication.

III. PERFORMANCE

A. Power
Vedic Multiplier has less number of gates required for given 8x8 bits Multiplier so its power dissipation is very small as compared to other multiplier architecture. Vedic Multiplier has less switching activity as compared to other architecture for same operation. The improvements are explained in the following steps 1-5.

- In parallel computation B of (a) square algo, the term X1*Y0+X0*Y1 of (2) multiplier algo, that is, two 4x4 multiply operations are reduced to 2* X1*X0, that is, one 4x4 multiply operation (and multiply by 2 requires only shift operation).
- In parallel computation C of (a) square algo, the term X2 * Y0+X0*Y2 + X1 * Y1 of (2) multiplier algo, that is, three 4x4 multiply operations are reduced to 2* X2 * X0+X1 * X1, that is, only two 4x4 bit operations.
- In parallel computation D of (a) square algo, the term X3 * Y0+X0*Y3+ X2 * Y1 +X1 * Y2 of (2) multiplier algo, that is, 4 multiply operations of 4x4 bit are reduced to 2 * X3 * X0+2 * X2 *X1, that is, only two multiply operations.
- In parallel computation E of (a) square algo, the term X3 * Y1 +X1 * Y3+X2 * Y2 of (2) multiplier algo, that is, three 4x4 multiply operations are reduced to 2 * X3 * X1 +X2 * Y2, that is, only two multiply operations.
- In parallel computation F of (a) square algo, the term X3*Y2+X2*Y3 of (2) multiplier algo, that is, two 4x4 bit multiply operations are reduced to 2 *X3 * X2, that is, only one multiply operation.

B. Speed
Vedic multiplier is faster than array multiplier and Booth multiplier. As the number of bits increases from 8x8 bits to 16x16 bits, the timing delay is greatly reduced for Vedic multiplier as compared to other multipliers. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Delay in Vedic multiplier for 16 x 16 bit number is 32 ns while the delay in Booth and Array multiplier are 37 ns and 43 ns respectively. Thus this multiplier shows the highest speed among conventional multipliers. It has this advantage than others to prefer a best multiplier.

C. Area
The area needed for Vedic square multiplier is very small as compared to other multiplier architectures i.e. the number of devices used in Vedic square multiplier are 259 while Booth and Array Multiplier is 592 and 495 respectively for 16 x 16 bit number when implemented on Spartan FPGA. Thus the result shows that the Vedic square multiplier is smallest and the fastest of the reviewed architectures. The Vedic square and cube architecture proved to exhibit improved efficiency in terms of speed and area compared to Booth and Array Multiplier. Due to its parallel and regular structure, this architecture can be easily realized on silicon and can work at high speed without increasing the clock frequency. It has the advantage that as the number of bits increases, the gate delay and area increase very slowly as compared to the square and cube architectures of other multiplier architecture. Speed improvements are gained by parallelizing the generation of partial products with their concurrent summations. It is demonstrated that this design is quite efficient in terms of silicon area/speed. Such a design should enable substantial savings of resources in the FPGA when used for image/video processing applications.

IV. RESULT

<table>
<thead>
<tr>
<th>Multiplication of a*b</th>
<th>Input a</th>
<th>Input b</th>
<th>Output c</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>9</td>
<td>7</td>
<td>63</td>
</tr>
</tbody>
</table>

Fig.2.

Multiplication of a*b
Input a = 13
Input b = 14
Output c = 182
Fig.3.
Schematic View
a and b are the inputs.
c is the output.
\textit{rst} is reset.

![Schematic View](image)

Fig.4.
A. Technology schematic: This shows the internal architecture of the top module. Which consist of LUTs, MUX etc

![Technology schematic](image)

Fig.5.

**V. CONCLUSION**

In this paper, a new architecture for a power efficient Vedic multiplier is presented. Simulation and synthesis are carried out for three different cases. The multipliers can be chosen depending on what the performance it is required. The proposed Vedic multiplier architecture shows good improvement in power consumption in third case. This multiplier can be efficiently used in any DSP application or in any DSP processors that requires low power consumption.

**VI. REFERENCES**


